



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/507,261	02/18/2000	Robert J. Safranek	2791-52913	9010

25253 7590 10/01/2002

IBM CORPORATION  
IP LAW DEPT, ED02-905  
15450 SW KOLL PARKWAY  
BEAVERTON, OR 97006-6063

EXAMINER

ELMORE, REBA I

ART UNIT PAPER NUMBER

2187

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS  
UNITED STATES PATENT AND TRADEMARK OFFICE  
WASHINGTON, D.C. 20231  
[www.uspto.gov](http://www.uspto.gov)

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Paper No. 9

Application Number: 09/507,261

Filing Date: February 18, 2000

Appellant(s): LAIS ET AL.

**MAILED**

OCT 01 2002

*Technology Center 2100*

Pryor A. Garnett  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed September 25, 2002

This is in response to the brief on appeal filed September 25, 2002.

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is substantially correct.

Arguments regarding the remote nodes not having cache directory is considered persuasive.

Claims 3, 16 and 19-20 are withdrawn from the rejection.

This appeal involves claims 1-2, 4-15 and 17-18.

**(4) *Status of Amendments After Final***

No amendment after final has been filed.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) *Grouping of Claims***

Appellant's brief includes a statement that claims 1-20 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

**(8)      *ClaimsAppealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,802,578 Lovett 9-98

## **(10) *Grounds of Rejection***

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-15 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lovett.

Lovett teaches the invention (claims 1, 10 and 14) as claimed including a multimode computer system and method having a distributed shared memory with a remote node receiving a copy of a cache line stored in a home node, the system and method comprising:

a first node having multiple processors, a local memory and a remote cache (e.g., see Figures 2 and 3);

a system interconnect coupling the first node to the second node (e.g., see Figures 2 and 3):

a state machine located on the second node (e.g., see Figure 5):

a second node having multiple processors, a local memory and a remote cache (e.g., see Figures 2-3);

a remote node requesting a shared copy of a cache line that is stored on a home node (e.g., see col. 4, line 57 to col. 5, line 6);

receiving at the remote node a request to invalidate the cache line (e.g., see Table 1 in col. 5);

in response to the request to invalidate the cache line requesting an exclusive copy of the cache line is taught as updating a cache line which is in a state indicating it is the ‘only cached copy’ either consistent with memory or inconsistent with memory (e.g., see col. 5, Table 1);

overwriting the cache line on the remote node without informing the home node that the cache line is no longer stored on the remote node (e.g., see col. 5, Table 1); and,

requesting a new copy of the cache line after overwriting the cache line (e.g., see col. 5, Table 1).

As to claim 2, Lovett teaches storing a shared copy of the cache line on the remote node and rolling out the cache line on the remote node prior to the request for a shared copy of the cache line without informing the home node of the rollout (e.g., see col. 5, Table 1).

As to claim 4, Lovett teaches issuing a request for the cache line from a processor of the home node at approximately the same time the request for the shared copy of a cache line is received from the remote node (e.g., see col. 8, lines 20-26).

As to claims 5 and 11, Lovett teaches discarding a response to the request for the shared copy of cache line after receiving the invalidate request (e.g., see col. 7, lines 18-48).

As to claim 6, Lovett teaches passing data between the nodes using a system interconnect that includes a dualport RAM controlled by at least one state machine (e.g., see Figure 3)

As to claim 7, Lovett teaches a state machine in the remote node which remains in a first pending state upon requesting a cache line (e.g., see col. 5, Table 1);

if while in the first pending state storing the cache line in a cache in the remote node and transitioning to a dirty or fresh state when receiving the cache line (e.g., see col. 5, Table 1);

if while in the first pending state transitioning to a second pending state when a request is invalid (e.g., see col. 5, Table 1); and,

while in the second pending state discarding the cache line and issuing the request for an exclusive copy of the cache line upon receiving the cache line (e.g., see col. 5, Table 1).

As to claim 8, Lovett teaches the multimode computer system includes multiple processors at each node arranged in an unordered network (e.g., see Figure 1).

As to claim 9, Lovett teaches the multimode computer system includes at least two nodes but it is inherent the system could be one two nodes (e.g., see Figure 1).

As to claim 12, Lovett teaches receiving a processor request on the home node for control of a cache line (e.g., see col. 7, lines 1-48);

checking local tags to determine if another node has a shared copy of the cache line (e.g., see col. 7, lines 1-48); and,

sending the invalidate request to the remote node because the home node was not notified that the remote node has overwritten its copy of the cache line upon determining another node has a shared copy (e.g., see col. 7, lines 1-48).

As to claim 13, Lovett teaches receiving an exclusive copy of the cache line at the remote node (e.g., see col. 5, Table 1).

As to claim 15, Lovett teaches snoopy cache protocol engines (e.g., see Figure 3).

As to claim 17, Lovett teaches the remote node performs silent rollouts of data (e.g., see col. 5, Table 1).

**(11) *Response to Argument***

Appellant states '*Lovett* describes sending invalidate requests to other nodes, but not receiving and processing such invalidate requests by those other nodes. In order to maintain a coherent memory system, the invalidate requests must receive appropriate processing. Not all the nodes will need to make an active response to the invalidate request. Stating that *Lovett* does not teach responding to a received invalidate request with a request for an exclusive copy is an over simplification of the activity. Multiple remote nodes may need to invalidate a copy of a requested cache line but only one remote node can be given exclusivity of the cache line. Only the remote cache requesting the cache line will be given this ability.

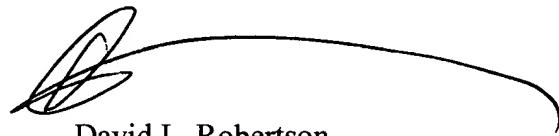
As to *Lovett* not teaching or suggesting skipping over the directory when determining the location of a memory block, this is not a claimed limitation. Appellant does not claim how the determination of a valid copy and its location is made, therefore the system and method taught by *Lovett* has not been precluded and is therefore valid.

Arguments concerning the limitation of remote nodes not have a cache directory are persuasive. These claims (claims 3, 16 and 19-20) are now considered allowable over the art of record.

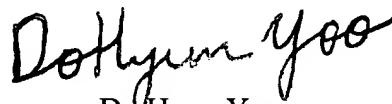
For the above reasons, it is believed that the rejection should be sustained.



Reba I. Elmore  
Primary Patent Examiner  
Art Unit 2187



David L. Robertson  
Primary Patent Examiner  
Art Unit 2187



Do Hyun Yoo  
Supervisory Patent Examiner  
Art Unit 2187